What is claimed is:

1. An electromagnetic digitizer sensor coupled to a processor, comprising:

a first array of sensing loops each coupled between the processor and a first potential node, each sensing loop in the first array being selectively connectable to the processor and further being selectively connectable to the first potential node.

2. The electromagnetic digitizer sensor of claim 1, wherein the first potential node is a ground node.

3. The electromagnetic digitizer sensor of claim 1, further including:

a substrate, wherein the first array of sensing loops are formed at a first level of the substrate; and

a second array of sensing loops each coupled between the processor and a second potential node, each sensing loop in the second array being switchable to connect and disconnect to the processor and further being switchable to connect and disconnect to the second potential node, the second array being formed on a second level of the substrate different from the first level.

4. The electromagnetic digitizer sensor of claim 3, wherein at least one of the first and second levels of the substrate are a surface of the substrate.

5. An electromagnetic digitizer sensor coupled to a processor, comprising:

a substrate having a first level; and

an array of sensing loops disposed completely at the first level, each of the sensing loops being selectably coupled between the processor and a potential node such that any one of the sensing loops can be selected to form a closed circuit between the processor and its respective node without being short-circuited by any of the other sensing loops.

6. The electromagnetic digitizer sensor of claim 5, wherein the potential node is a ground node.

7. The electromagnetic digitizer sensor array of claim 5, wherein the array of sensing loops are indium tin oxide and the substrate is glass.

8. An electromagnetic digitizer sensor, comprising:

a substrate having first and second different levels;

an array of first sensing loops each disposed at the first level but not the second level; and

an array of second sensing loops each disposed at the second level but not the first level.

9. The electromagnetic digitizer sensor of claim 8, wherein the first sensing loops are arranged in a comb-like pattern and the second sensing loops are arranged in a comb-like pattern.

10. The electromagnetic digitizer sensor of claim 8, integrated with a display.

11. An electromagnetic digitizer sensor coupled to a processor, comprising:

a first plurality of sensing traces electrically coupled in parallel between the processor and a first node;

a second plurality of sensing traces electrically coupled in parallel between a second node and the first node;

a first plurality of switches each coupled between one of the first plurality of sensing traces and the processor; and

a second plurality of switches each coupled between one of the second plurality of sensing paths and the second node.

12. The electromagnetic digitizer sensor of claim 11, wherein the second node is a ground node.

13. The electromagnetic digitizer sensor of claim 11, wherein the first node is a floating node.

14. The electromagnetic digitizer sensor of claim 11, wherein the first plurality of sensing traces are disposed so as to be interleaved with the second plurality of sensing traces.

15. The electromagnetic digitizer sensor of claim 11, wherein the first plurality of switches are embodied as a multiplexor.

16. The electromagnetic digitizer sensor of claim 11, wherein the first plurality of sensing traces are further switchably connectable to the second node and the second plurality of sensing traces are further switchably connectable to the processor.

17. The electromagnetic digitizer sensor of claim 11, wherein the first and second plurality of sensing traces are arranged in a comb-like pattern.

18. The electromagnetic digitizer sensor of claim 11, wherein the first and second plurality of sensing traces are each arranged to be physically parallel with each other.

19. The electromagnetic digitizer sensor of claim 11, wherein the first and second plurality of switches are each single-pole-single-throw switches.